Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously presented) A method of forming a transistor having source and drain regions within a substrate adjacent a gate stack on the substrate, comprising:

forming a layer of poly-SiGe with carbon over a dielectric layer situated on the substrate;

forming a polysilicon seed layer over the dielectric layer;

forming a layer of poly-Si over the layer of poly-SiGe; and

patterning the poly-Si, poly-SiGe and dielectric layers to form the gate stack; wherein the polysilicon seed layer is patterned in forming the gate stack.

2. (Original) The method of claim 1, wherein the layer of poly-Si includes carbon.

3. (Cancelled)

4. (Previously presented) The method of claim 1, wherein the seed layer includes carbon.

5. (Original) The method of claim 4, wherein the poly-Si, poly-SiGe and seed layers are patterned *via* an etching process.

6. (Original) The method of claim 5, wherein the carbon within the layers changes a passivation material formation and etch rate during the etching process.

7. (Original) The method of claim 6, wherein the etching is substantially isotropic due to the change in passivation and etch rate.

8. (Original) The method of claim 7, wherein the poly-SiGe layer has a greater etch sensitivity to an etchant utilized to etch the layers in forming the gate structure.

9. (Original) The method of claim 8, wherein at least one of the seed layer, poly-SiGe layer and poly-Si layer contains a concentration of carbon between about 0.1 to 1.0 atomic percent.

10. (Previously presented) The method of claim 1, wherein the seed layer has a thickness of about 100 Angstroms or less.

11. (Original) The method of claim 1, wherein the poly-SiGe layer has a thickness of about 400 to 700 Angstroms.

12. (Original) The method of claim 1, wherein the poly-Si layer has a thickness of about 350 to 750 Angstroms.

13. (Original) The method of claim 1, wherein the dielectric layer has a thickness of about 100 Angstroms.

14. (Original) The method of claim 4, wherein at least one of the dielectric layer, seed layer, poly-SiGe layer and poly-Si layer is formed according to at least one of spin-on techniques, sputtering techniques, growth techniques and deposition techniques.

15-19. (Cancelled)

20. (Previously presented) A method of forming a transistor, comprising:

forming a layer of dielectric material over a substrate;

forming a layer of poly-SiGe with carbon over a dielectric layer situated on the substrate;

forming a layer of poly-Si over the layer of poly-SiGe;

patterning the poly-Si, poly-SiGe and dielectric layers to form a gate stack; doping exposed portions of the substrate adjacent to the gate stack to form source and drain regions;

forming a polysilicon seed layer over the layer of dielectric material; and

patterning the polysilicon seed layer in forming the gate stack.

21. (Cancelled) The method of claim 15, wherein the layer of poly-Si includes carbon.

22. (Previously presented) A method of forming a transistor, comprising:

forming a layer of dielectric material over a substrate;

forming a layer of poly-SiGe with carbon over a dielectric layer situated on the substrate;

forming a layer of poly-Si over the layer of poly-SiGe, wherein the layer of poly-Si includes carbon;

patterning the poly-Si, poly-SiGe and dielectric layers to form a gate stack;

doping exposed portions of the substrate adjacent to the gate stack to form source and drain regions;

forming a polysilicon seed layer over the dielectric layer; and

patterning the polysilicon seed layer in forming the gate stack.

23. (Original) The method of claim 22, wherein the seed layer includes carbon.

24. (Original) The method of claim 23, wherein the poly-Si, poly-SiGe and seed layers are patterned *via* an etching process, and wherein the poly-SiGe layer has a greater etch sensitivity to an etchant utilized to etch the layers.

25. (Original) The method of claim 23, wherein at least one of the seed layer, poly-SiGe layer and poly-Si layer contains a concentration of carbon between about 0.1 to 1.0 atomic percent.

26. (Original) The method of claim 22, wherein the seed layer has a thickness of about 100 Angstroms or less.

27-44 (canceled).